AMENDMENTS

Listing of Claims

This listing of claims replaces all prior versions and listings of claims in the application.

1. (Currently amended) A system for generating amplitude matched, phase shifted signals, comprising:

a filter arrangement including a plurality of input and output nodes, a first set of input nodes arranged to receive an input signal, a second set of input nodes coupled to electrical ground, each output node configured to provide an associated vector that is offset in phase from a vector associated with each other output node; and

an adjustable element associated with each output node, the adjustable element configured to receive a feedback signal and in response to the feedback signal substantially equalize an amplitude of each vector associated with each output node.

2. (Currently amended) The system of claim 1, wherein four output nodes are associated with the filter arrangement, each output node having an associated vector.

3. (Original) The system of claim 2, further comprising:

an adder element configured to add the four vectors resulting in eight phase shifted vectors.

4. (Original) The system of claim 3, further comprising:

a scaler configured to scale the amplitude of the four vectors resulting in eight amplitude matched phase shifted vectors.

5. (Original) The system of claim 4, wherein the adjustable element is an adjustable resistance.

6. (Original) The system of claim 5, wherein the adjustable resistance is a metal oxide semiconductor field effect transistor (MOSFET) adjustable resistance.

7. (Original) The system of claim 4, wherein the adjustable element is an adjustable capacitance.

8. (Original) The system of claim 7, wherein the adjustable capacitance is a varactor.

9. (Currently amended) A method for generating amplitude matched, phase shifted signals, comprising:

providing a plurality of vectors, each vector associated with a respective output node, each vector offset in phase from each other vector associated with each other output node;

applying an input signal at a subset of a set of input nodes;

providing a feedback signal to a respective adjustable element associated with each input and output node; and

adjusting each ~~node~~ adjustable element using the feedback signal to substantially equalize an amplitude of each vector associated with each output node.

10. (Currently amended) The method of claim 9, wherein a resistance associated with each output node is adjusted to substantially equalize an amplitude of each vector associated with each output node.

11. (Currently amended) The method of claim 9, wherein a capacitance associated with each output node is adjusted to substantially equalize an amplitude of each vector associated with each output node.

12. (Original) The method of claim 10, further comprising adjusting the resistance using a metal oxide semiconductor field effect transistor (MOSFET) adjustable resistance.

13. (Currently amended) The method of claim 12, further comprising combining four vectors associated with each of four output nodes resulting in eight phase shifted vectors.

14. (Original) The method of claim 13, further comprising scaling the four vectors resulting in eight substantially amplitude matched phase shifted vectors.

15. (Original) The method of claim 11, further comprising adjusting the capacitance using a varactor.

16. (Currently amended) The method of claim 15, further comprising combining four vectors associated with each of four output nodes resulting in eight phase shifted vectors.

17. (Original) The method of claim 16, further comprising scaling the four vectors resulting in eight amplitude matched phase shifted vectors.

18. (Currently amended) A system for generating amplitude matched, phase shifted signals, comprising:

filter means including a plurality of input and output nodes, a first set of input nodes arranged to receive an input signal, a second set of input nodes coupled to electrical ground, the filter means for providing a plurality of associated vectors that are offset in phase from each other vector associated with each other output node;

means for providing a feedback signal to an adjustable element associated with each output node; and

means for using the feedback signal to substantially equalize an amplitude of each vector associated with each output node.

19. (Original) The system of claim 18, wherein the means for substantially equalizing an amplitude of each vector comprises adjustable resistance means.

20. (Original) The system of claim 18, wherein the means for substantially equalizing an amplitude of each vector comprises adjustable capacitance means.

21. (Original) The system of claim 19, wherein the adjustable resistance means comprises a metal oxide semiconductor field effect transistor (MOSFET) adjustable resistance.

22. (Currently amended) The system of claim 21, further comprising:

adder means for combining four vectors associated with each of four output nodes resulting in eight phase shifted vectors.

23. (Original) The system of claim 22, further comprising:

scaler means for scaling an amplitude of the four vectors resulting in eight substantially amplitude matched phase shifted vectors.

24. (Currently amended) A system for generating amplitude matched, phase shifted signals, in a portable communication device, comprising:

a portable communication device including a transmitter and a receiver;

a synthesizer for providing a local oscillator signal;

a filter arrangement configured to operate on the local oscillator signal, the filter arrangement including a plurality of input and output nodes, a first set of input nodes arranged to receive the local oscillator signal, a second set of input nodes coupled to electrical ground, each output node configured to provide an associated vector that is offset in phase from a vector associated with each other output node; and

an adjustable element associated with each output node, the adjustable element configured to receive a feedback signal and in response to the feedback signal substantially equalize an amplitude of each vector associated with each output node.

25. (Currently amended) The system of claim 24, wherein four output nodes are associated with the filter arrangement, each output node having an associated vector.

26. (Original) The system of claim 25, further comprising:

an adder element configured to add the four vectors resulting in eight phase shifted vectors.

27. (Original) The system of claim 26, further comprising:

a scaler configured to scale an amplitude of the four vectors resulting in eight substantially amplitude matched phase shifted vectors.

28. (Original) The system of claim 27, wherein the adjustable element is an adjustable resistance.

29. (Original) The system of claim 28, wherein the adjustable resistance is a metal oxide semiconductor field effect transistor (MOSFET) adjustable resistance.

30. (Original) The system of claim 27, wherein the adjustable element is an adjustable capacitance.

31. (Original) The system of claim 30, wherein the adjustable capacitance is a varactor.